REMARKS

Present Status of the Application

Claims 1-11 are still pending in the present invention. Claim 4 is amended as indicated in the first paragraph of the OFFICE ACTION, claims 1 and 11 are amended and new claim 12 is added. It is believed that no new matter is introduced from the amendments. Applicant respectfully traverses the rejections set forth in the Office Action for at least the reasons below. Applicant respectfully disagrees with the rejections and reconsideration of this application is respectfully requested.

Discussion for rejection to claims under 35 U. S. C. 102(b)

Claim 11 is rejected under 35 U .S. C. 102(b) as being anticipated by Chen et al. (US patent no. 6,351,364, "Chen" hereinafter).

In response thereto, Applicants respectfully traverses the rejections based on the following arguments and thus withdrawal of rejections addressed to claim 11 is respectfully requested.

For a proper rejection of a claim under 35 U.S.C. Section 102(b), the cited reference must disclose all features of the claim.

Independent claim 11, as amended, states:

> An electrostatic discharge (ESD) protection circuit coupled to a pad of an integrated circuit, the integrated circuit having a system voltage and a ground voltage, the ESD protection circuit comprising:
>
> a P-type transistor, a first S/D terminal and a gate terminal of the P-type transistor coupled to the system voltage, a second S/D terminal of the P-type transistor coupled to the pad;
>
> a first N-type transistor, **a first S/D terminal of the first N-type transistor directly coupled to the system voltage**, a gate terminal of the first N-type transistor coupled to the ground voltage, a second S/D terminal of the first N-type transistor coupled to the pad; and
>
> a second N-type transistor, a first S/D terminal of the second N-type transistor coupled to the pad, a gate terminal and a second S/D terminal of the second N-type transistor coupled to the ground voltage.

Independent claim 11 is allowable for at least the reason that Chen does not disclose, teach, or suggest the features that are highlighted in claim 11 above. More specifically, Chen does not disclose, teach, or suggest the feature of "a first S/D terminal of the first N-type transistor directly coupled to the system voltage" in the ESD protection circuit of claim 11 of

present invention.

In the office Action, the NMOS transistor 40 in Fig.2 of Chen is asserted be the "first N-type transistor" and the NMOS transistor 38 in Fig. 2 of Chen is asserted to the "second N-type transistor." Applicant does not agree with such assertions because that the ESD circuit 30 in Fig.2 of Chen is not equivalent and different from the subject matter of claim 11 in the present invention. The NMOS transistor 40 in Fig.2 of Chen is coupled to the system voltage VDD through a resistor 46, not directly coupled to the system voltage VDD. By such arrangement, the NMOS transistor 40 in Fig.2 of Chen is used as a coupling circuit, not for the ESD bypass circuit. The NMOS transistors 40 and 42 in Fig. 2 of Chen are used as the coupling circuit to trigger the NMOS transistor 38 to be an ESD bypass path in the negative stress condition, *See Col. 4, Lines 16-43 of the Chen.*

However, the first S/D terminal of the first N-type transistor is directly coupled to the system voltage, which is used as an ESD bypass path for the ESD protection circuit. The NMOS transistor 40 in Fig.2 of Chen is not equivalent and different from the first N-type transistor of the invention.

Thus, Chen does not anticipate claim 11, and the rejection should be withdrawn.

If independent claim 11 is allowable over the prior art of record, then its dependent claim 12 is allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 11. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Additionally and notwithstanding the foregoing reasons for the allowability of claim 11, the dependent claim 12 recite further features that are patentably distinct from the prior art of record. The claim 12 recites that the ESD protection circuit further comprises a diode, a cathode of the diode coupled to a common conductive line, an anode of the diode coupled to the system voltage. By coupling to the common conductive line through a diode, the electrostatic discharge (ESD) protection circuit is adapted to serve ESD protection of a single-power system or a multi-power system, which is not disclosed, taught, or suggested in the references of record. Hence, there are other reasons why the dependent claim 12 is allowable.

Discussion for rejection to claims 1-6 under 35 U. S. C. 103(a)

Claims 1-2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Okitaka (U.S. Patent No. 4,858,055, "Okitaka" hereinafter).

In response thereto, Applicants respectfully traverses the rejections based on the

following arguments and thus withdrawal of rejections addressed to claims 1-2 is respectfully requested.

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all elements/features/steps of the claim at issue. See, *e.g.*, *In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

Independent claim 1, as amended, recites the following:

1. An electrostatic discharge (ESD) protection circuit coupled to a first pad of an integrated circuit, the integrated circuit having a plurality of system voltage sets, the system voltages including a first system voltage and a first ground voltage, the ESD protection circuit comprising:

a first common conductive line;

a first diode, a cathode of the first diode coupled to the first common conductive line, an anode of the first diode coupled to the first system voltage;

a first P-type transistor, a first S/D terminal and a gate terminal of the first P-type transistor coupled to the first system voltage, a second S/D terminal of the first P-type transistor coupled to the first pad; and

a first N-type transistor, a first S/D terminal of the first N-type transistor directly coupled to the first common conductive line, a gate terminal of the first N-type transistor coupled to the first ground voltage, a second S/D terminal of the first N-type transistor coupled to the first pad.

Dependent claim 2 recites the following:

...further comprising a second N-type transistor, a first S/D terminal of the second N-type transistor coupled to the first pad, a gate terminal and a second S/D terminal of the second N-type transistor coupled to the first ground voltage.

Chen

As explained above, the first S/D terminal of the first N-type transistor is directly coupled to the first common conductive line, which is used as an ESD bypass path for the ESD protection circuit in the present invention. However, the NMOS transistor 40 in Fig.2 of Chen, upon which the Office Action relied, is not equivalent and different from the first N-type transistor of the invention. The NMOS transistors 40 and 42 in Fig. 2 of Chen is used as the coupling circuit to trigger the NMOS transistor 38 to be an ESD bypass path in the negative stress condition, *See Col. 4, Lines 16-43 of the Chen.*, not as the ESD bypass path as claimed.

In addition, as admitted in the Office Action, Chen does not teach connecting a diode in series with the PFET. The Office Action referred extensively to the passages (Figure 2) of Okitaka relating to the "a first diode, a cathode of the first diode coupled to the first common conductive line, an anode of the first diode coupled to the first system voltage" as claimed. More particularly, the Office Action referred to the passages that, in Figure 2 of Okitaka, the diode (3) in series with a PFET (12) and power, where the cathode is coupled to the power and the anode is coupled to the PFET, and asserted that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Chen with Okitaka by placing a diode in series with the first PFET for the purpose of preventing current flow through the PFET (44) to the internal circuitry when a surge voltage is not present.

Okitaka

First of all, please refer to Okitaka, "a control circuit 20 for controlling an on-off operation of the P-channel MOS transistor 12 in response to the voltage applied to the first power supply terminal 8" (See col.3, ll 46-49). As also stated in Col. 5, Lines 26-31 and Lines 35-40,

> "an input voltage can be clamped to the level of "(V_{CC} +V_F +V_{TH})" by the input clamping diode 3 even if an overvoltage higher than the supply potential V_{CC} is applied to the signal input terminal 1 when the operation supply potential V_{CC} is applied to the first power supply terminal 8."
>
> "an input voltage is clamped to the level of " (a ground potential- V_F)" by the input clamping diode 4 in case that a voltage lower than a ground potential is applied to the signal input terminal 1 when the supply potential V_{CC} is applied to the first power supply terminal 8."

In the "Input Protecting Device" of the Okitaka, only the diode (3) is used, in the case that the P-channel MOS transistor 12 is turned on, for protection if an overvoltage higher than the supply potential V_{CC} is applied to the signal input terminal 1 when the operation supply potential V_{CC} is applied to the first power supply terminal 8. Only the diode (4) is used for protection if a voltage lower than a ground potential is applied to the signal input terminal 1 when the supply potential V_{CC} is applied to the first power supply terminal 8.

However, in the present invention, if a positive ESD pulse is charged to the pad 350a, the P-type transistor 330a, the diode 370 and the N-type transistor 340b for multi-power protection are used for ESD protection. If a negative ESD pulse is charged to the pad 350a,

the N-type transistor 340a and the N-type transistor 340b for multi-power protection are used for ESD protection.

The combination of Chen in view of Okitaka fails to establish a *prima facie* case of obviousness

Independent claim 1 is allowable for at least the reason that the combination of Chen in view of Okitaka at least does not disclose, teach, or suggest the features that "a first diode, a first P-type transistor and a first N-type transistor" as claimed in claim 1, and further "a second N-type transistor" as claimed in claim 2.

Chen or Okitaka, alone or combined, does not disclose, teach, or suggest, either implicitly or explicitly, all elements/features/steps of the claim at issue. For example, Chen or Okitaka, alone or combined, does not disclose, teach, or suggest, either implicitly or explicitly, that "the first S/D terminal of the first N-type transistor is directly coupled to the first common conductive line", which is used as an ESD bypass path for the ESD protection circuit in the present invention.

In addition, Chen or Okitaka, alone or combined, does not disclose, teach, or suggest, either implicitly or explicitly, that "a first diode, a cathode of the first diode coupled to the first common conductive line, an anode of the first diode coupled to the first system voltage", as claimed. The Office Action refers extensively to the diode (3) in series with a PFET (12) relating to the diode as claimed. However, it is respectfully submitted that the Examiner's interpretation of the cited reference is somewhat overreaching. As stated above, the diode (3) in Okitaka is used, in the case that the P-channel MOS transistor 12 is turned on, for protection if an overvoltage higher than the supply potential V_{CC} is applied to the signal input terminal 1 when the operation supply potential V_{CC} is applied to the first power supply terminal 8. Okitaka does not disclose the diode, which the cathode of the diode coupled to the first common conductive line, an anode of the diode coupled to the first system voltage, as claimed in claim 1, for the multi-power ESD protection in the present invention.

Thus, a prima facie case of obviousness is not well established. The combination of Chen in view of Okitaka, and further in view of Miller, does not render claims 1 and 2 obvious, and the rejection should be withdrawn.

Because independent claim 1 is allowable over the prior art of record, its dependent claims 3-6 are allowable as a matter of law, for at least the reason that these dependent claims

contain all features/elements/steps of their respective independent claim 1. Additionally and notwithstanding the foregoing reasons for the allowability of claim 1, these dependent claims recite further features/steps and/or combinations of features that are patentably distinct from the prior art of record. Hence, there are other reasons why these dependent claims are allowable. For example, dependent claim 4 recites the ESD protection circuit is coupled to a second pad of the integrated circuit. The ESD protection circuit further comprises a fourth diode, a second P-type transistor, and a third N-type transistor. The electrostatic discharge (ESD) protection circuit adapted to serve ESD protection of **multi-power system and input/output pins** and to discharge the ESD pulse for protecting internal circuits.

Discussion for rejection to claims under 35 U. S. C. 103(a)

Claims 7-8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Okitaka, and further in view of Miller (U.S. Patent No. 6,327,126, "Miller" hereinafter)..

In response thereto, Applicants respectfully traverses the rejections based on the following arguments and thus withdrawal of rejections addressed to claims 7-8 is respectfully requested.

Independent claim 7, as amended, recites the following:

> An electrostatic discharge (ESD) protection circuit coupled to a first pad of an integrated circuit, the integrated circuit having a plurality of system voltage sets, the system voltages including a first ground voltage, the ESD protection circuit comprising:
> a first common conductive line;
> *a first diode, a cathode of the first diode coupled to the first ground voltage, an anode of the first diode coupled to the first common conductive line*; and
> *a first N-type transistor, a first S/D terminal of the first N-type transistor coupled to the first pad, a gate terminal and a substrate terminal of the first N-type transistor coupled to the first ground voltage, a second S/D terminal of the first N-type transistor coupled to the first common conductive line.*

As the same reasons set forth above, Chen or Okitaka, alone or combined, does not disclose, teach, or suggest, either implicitly or explicitly, that "*a first N-type transistor, a first S/D terminal of the first N-type transistor coupled to the first pad, a gate terminal and a substrate terminal of the first N-type transistor coupled to the first ground voltage, a second S/D terminal of the first N-type transistor coupled to the first common conductive line*" "*a first diode, a cathode of the first diode coupled to the first ground voltage, an anode of the first diode coupled to the first common conductive line*;

In addition, referring to item 10, on page 5 of the Office Action, it is asserted that, in Chen, the other S/D terminal of the PFET (44) is connected to a first voltage, and the second S/D terminal of the NFET (40) is connected to a second voltage. However, both of these two S/D terminals, as shown in FIG 2, are connected to the same voltage VDD.

Thus, a prima facie case of obviousness is not well established. The combination of Chen in view of Okitaka, and further in view of Miller, does not render claims 7 and 8 obvious, and the rejection should be withdrawn.

Because independent claim 7-8 is allowable over the prior art of record, its dependent claims 9-10 are allowable as a matter of law, for at least the reason that these dependent claims contain all features/elements/steps of their respective independent claim 7. Additionally and notwithstanding the foregoing reasons for the allowability of claim 7, these dependent claims recite further features/steps and/or combinations of features that are patentably distinct from the prior art of record. Hence, there are other reasons why these dependent claims are allowable. For example, dependent claim 9 recites the ESD protection circuit is coupled to a second pad of the integrated circuit, the plurality of system voltage sets further comprises a second ground voltage, and the ESD protection circuit further comprises a third diode, a cathode of the third diode coupled to the second ground voltage, an anode of the third diode coupled to the first common conductive line; and a third N-type transistor, a first S/D terminal of the third N-type transistor coupled to the second pad, a gate terminal and a substrate terminal of the third N-type transistor coupled to the second ground voltage, a second S/D terminal of the third N-type transistor coupled to the first common conductive line. The electrostatic discharge (ESD) protection circuit adapted to serve ESD protection of **multi-power system and input/output pins** and to discharge the ESD pulse for protecting internal circuits.

Customer No.: 31561
Application No.: 10/707,870
Docket No.: 12049-US-PA

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-12 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Jan. 26, 2006

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